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SYSTEM:OS  - DIALOG OneSearch
  File 350:Derwent WPIX  1963-2001/UD,UM &UP=200215
        (c) 2002 Derwent Info Ltd
*File 350: Price changes as of 1/1/02. Please see HELP RATES 350.
More updates in 2002.  Please see HELP NEWS 350.
  File 347:JAPIO  Oct/1976-2001/Nov(Updated 020305)
        (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
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Set	Items	Description
S1	386888	TUNGSTEN OR W OR WOLFRAM
S2	487814	SILICON OR SI
S3	143	SILICON(2N)INSULATOR() METAL() OXIDE()SEMICONDUCTOR OR SOI-(W) MOSFET
S4	2508703	TRENCH?? OR HOLE? ? OR GROOVE? ? OR CHANNEL? ? OR EDGE? OR FLUSH OR RIDGE?
S5	29327	(EPI OR EPITAX?)(3N)(LAYER? OR FILM OR FILMS OR COAT????)
S6	7442	(BURY??? OR BURIED OR ENCAPSUL? OR CAPSUL? OR ENCAS?????)(-3N)(INSULAT? OR DIELECTRIC OR OXIDE)
S7	234118	DRAIN? ? OR DRIFT? ? OR (ACTIVE OR DIFFUSION OR SOURCE)(2N-)(REGION OR REGIONS OR AREAS OR AREA OR ZONE OR ZONES)
S8	568873	(INSULAT? OR DIELECTRIC OR OXIDE)(3N)(FILM? ? OR LAYER? OR COAT???? OR OVERCOAT???? OR MATERIAL? OR COVER???? OR MULTILA-YER? OR MULTI(W)LAYER?)
S9	411872	GATE? ? OR MEMORY()CELL OR LIBRARY()CELL
S10	2089537	(METAL? OR POLYSILICON)
S11	96	S3 AND (S1 OR S2)
S12	16	S11 AND S6
S13	76	S11 AND S8
S14	56	S13 AND S9
S15	43	S14 AND S7
S16	30	S15 AND S4
S17	20	S16 AND S10
S18	16	S17 NOT S12
S19	20	S3 AND S6
S20	4	S19 NOT (S12 OR S18)
S21	101	S3 AND S8
S22	73	S21 AND S7
S23	56	S22 AND S9
S24	13	S14 NOT S23
S25	11	S24 NOT (S12 OR S18 OR S20)
S26	69	S3 AND S10
S27	0	S26 AND S5
S28	52	S26 AND (S6 OR S8)
S29	40	S28 AND S7
S30	30	S29 AND S4
S31	10	S30 NOT S16
S32	8	S31 NOT (S12 OR S18 OR S20 OR S25)

12/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014111630
WPI Acc No: 2001-595842/200167
XRAM Acc No: C01-176411
XRPX Acc No: N01-444102
Silicon-on-insulator substrate for **silicon**-on-**insulator** **metal-oxide-semiconductor** field effect transistor, comprises conductive layers formed at through holes of **buried oxide** layer for body contacts of thin layer
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010025991	A1	20011004	US 2001803309	A	20010309	200167	B

Abstract (Basic): US 20010025991 A1
Abstract (Basic):
NOVELTY - A **silicon**-on-insulator (SOI) substrate comprises a **monosilicon** substrate (30) laminated with a **buried oxide** layer (42), on the surface. A thin **monosilicon** layer (41) is formed over entire surface of the **buried oxide** layer. Conductive layers are formed at through holes of the **buried oxide** layer positioned between the predetermined regions of thin layer and the substrate for body contacts.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) SOI substrate fabrication method;
(b) SOI metal-oxide-semiconductor field effect transistor (**SOI MOSFET**)

12/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013773979
WPI Acc No: 2001-258190/200126
XRAM Acc No: C01-077890
XRPX Acc No: N01-184139
Semiconductor device with graded top oxide and graded drift region, e.g. MOSFET or diode, is prepared by a process involving forming an oxidation mask on a thin semiconductor film and patterning the mask with openings
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG)
Inventor: LETAVIC T; SIMPSON M
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200124250	A1	20010405	WO 2000EP9403	A	20000925	200126	B
US 6221737	B1	20010424	US 99408786	A	19990930	200130	
EP 1142011	A1	20011010	EP 2000969307	A	20000925	200167	
			WO 2000EP9403	A	20000925		

Abstract (Basic): WO 200124250 A1

03/08/2002

Abstract (Basic):

NOVELTY - Lateral structure includes at least two semiconductor regions separated by a lateral drift region. A portion of a top oxide insulating layer over the thin semiconductor film increases continuously, and a portion of lateral drift region below the top oxide layer decreases in thickness continuously, both over a distance at least greater than maximum semiconductor film thickness by a factor of 5.

DETAILED DESCRIPTION - Semiconductor device (10) has a semiconductor substrate (100), a thin **buried oxide** **insulating** layer (102) on the substrate, and a lateral semiconductor device provided in a thin semiconductor film (104) on the thin **buried oxide**. The thin semiconductor film comprises a first conductivity-type region (106), a second, different, conductivity-type region (108) spaced apart from the first region (106) by a lateral drift region (110) of the second conductivity type.

A top insulating layer (112) is provided over the thin semiconductor film, and a conductive field plate (114) is provided on the top oxide insulating layer (112).

The top insulating layer (112) comprises a layer portion (112b) adjacent the first region (106) that increases in thickness in a substantially continuous manner in a direction from the first region toward the second region over a distance of at least about a factor of five greater than a maximum thickness of the thin semiconductor film.

The lateral drift region comprises a region portion (110a) adjacent the first region (106) that decreases in thickness in a substantially continuous manner in a direction from the first region toward the second region over the said distance.

Production of the semiconductor device, especially a MOSFET, includes:

(a) forming an oxidation mask comprising **silicon** nitride on the thin semiconductor film (104);

(b) patterning a portion of the mask with a series of sequential openings of different widths, a portion of the openings having a width less than a maximum thickness of a top oxide insulation layer; and

(c) thermally oxidizing the thin semiconductor film (104) using the mask to grow the top oxide insulation layer (112) with the layer portion (112b) that increases in thickness and to form the lateral drift region (110) with the region portion (110a) that decreases in thickness.

USE - Production of a semiconductor device such as a diode or a MOSFET, including SOI devices, suitable for high voltage and power applications.

ADVANTAGE - The device has improved performance since permissible saturated current flow is increased and the on resistance of the device structure is reduced, while maintaining high breakdown voltage capability. The device is produced by a relatively simple, economical and rapid process.

DESCRIPTION OF DRAWING(S) - The drawing shows a simplified cross-sectional view of a lateral **SOI MOSFET** device made in accordance with a first embodiment of the invention.

12/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013278889
WPI Acc No: 2000-450824/200039
XRPX Acc No: N00-335568

03/08/2002

3D electrostatic discharge structure formation for semiconductor and microelectronic field, involves forming discharge network on bulk substrate, which is connected to input pin and integrated structure
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: VOLDMAN S H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6074899	A	20000613	US 97833364	A	19970404	200039 B
			US 99245488	A	19990205	

Abstract (Basic): US 6074899 A
Abstract (Basic):
NOVELTY - A thin **silicon** film is separated from a bulk **silicon** substrate (40) by a **buried oxide** layer (42). An ESD network is formed on the substrate and on IC structure is formed on the thin film above the network. The network is then converted to an input pin (107).
DETAILED DESCRIPTION - During formation of ESD network, a bulk diode (102) is formed below thin film **SOI MOSFET** (104) of IC structure.

12/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012756927
WPI Acc No: 1999-563045/199948
XRAM Acc No: C99-164411
XRPX Acc No: N99-416052
Semiconductor device especially an **SOI MOSFET**
Patent Assignee: LG SEMICON CO LTD (GLDS); GOLDSTAR ELECTRON CO LTD (GLDS); HYUNDAI MICROELECTRONICS CO LTD (HYUN-N); HYUNDAI MICROSEMICON CO LTD (HYUN-N); HYUNDAI ELECTRONICS IND CO LTD (HYUN-N)
Inventor: HWANG J M; SON J H; HWANG J; SON J; SOHN J H
Number of Countries: 005 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19900992	A1	19991007	DE 1000992	A	19990113	199948 B
JP 11297854	A	19991029	JP 98357561	A	19981216	200003
KR 99079189	A	19991105	KR 9811669	A	19980402	200052
US 6218248	B1	20010417	US 99285258	A	19990402	200123
US 20010000411	A1	20010426	US 99285258	A	19990402	200124
			US 2000741439	A	20001221	

Abstract (Basic): DE 19900992 A1
Abstract (Basic):
NOVELTY - A semiconductor device has charge carrier discharge electrodes (B1, B2) for discharging charge carriers produced by impact ionization in transistors.
DETAILED DESCRIPTION - A semiconductor device has:
(a) first and second impurity ion implantation layers (32, 36) of predetermined conductivity type in a semiconductor substrate having a **buried oxide** film (22) and overlying **silicon** layers (23);
(b) first and second transistors of predetermined conductivity type on the respective first and second impurity ion implantation layers;
(c) trenches between the transistors;
(d) single crystal **silicon** layers (33, 37) formed on the trench side walls and connected to the transistor source/drain regions

and to the first and second impurity ion implantation layers; and
(e) charge carrier output electrodes (B1, B2) connected to the first and second impurity ion implantation layers at one of the transistor sides for output of charge carriers produced by impact ionization in the transistors. An INDEPENDENT CLAIM is also included for production of the above device.

12/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012363329
WPI Acc No: 1999-169436/199915
XRAM Acc No: C99-049750
XRPX Acc No: N99-123583
Silicon-on-insulator metal oxide field effect transistor
Patent Assignee: SHARP KK (SHAF)
Inventor: ADAN A O J; ADAN A O
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 902482	A1	19990317	EP 98305138	A	19980629	199915	B
JP 11087719	A	19990330	JP 97241482	A	19970905	199923	
KR 99029240	A	19990426	KR 9826541	A	19980702	200028	
US 6288425	B1	20010911	US 9899107	A	19980618	200154	

Abstract (Basic): EP 902482 A1
Abstract (Basic):
NOVELTY - A **silicon**-on-insulator metal oxide field effect transistor (**SOI-MOSFET**) has a region (6) embedded in the channel region which is separated from the source and drain regions (13).
DETAILED DESCRIPTION - A **SOI-MOSFET** comprises a semiconductor layer (3) on a **buried oxide** film (2) on a substrate (1) with a gate oxide film (7) and gate electrode (4) on the semiconductor film. There are oppositely doped source/drain regions (13) on both sides of the gate electrode and an oppositely doped embedded region (6) in the semiconductor layer which is separated from source/drain regions and from the semiconductor/gate oxide interface. An INDEPENDENT CLAIM also included for a process of forming the **SOI-MOSFET** comprising forming a deep doped channel by tilted ion implantation using the gate electrode as a mask to form the embedded region.
USE - In forming SOI-MOSFETS
ADVANTAGE - The problem of the kink effect is overcome, giving better control of parameters and increased yield: the area needed for the device can be reduced.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the **SOI-MOSFET**.

12/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012337160
WPI Acc No: 1999-143267/199912
XRPX Acc No: N99-104081
Semiconductor device where substrate floating effect is eliminated
Patent Assignee: HITACHI LTD (HITA)
Inventor: HORIUCHI M
Number of Countries: 023 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9905715	A1	19990204	WO 98JP3249	A	19980721	199912	B
JP 11040811	A	19990212	JP 97196206	A	19970722	199917	

Abstract (Basic):
NOVELTY - Semiconductor device has a source and drain symmetrical structure for each of pMOS and nMOS which eliminates substrate-floating effect.
DETAILED DESCRIPTION - An **SOI-MOSFET** has a mono crystal **silicon** layer (3) as a minority carrier path secured among the source-drain (9,10) and a **buried oxide** film (2) with a recombination center region (20) formed under an opening (19) for connecting the source and drain in order to get rid of minority carriers in this region.

12/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011895874
WPI Acc No: 1998-312784/199827
XRAM Acc No: C98-096576
XRPX Acc No: N98-245133
Semiconductor device - has isolation structure in which FS plate faces area of SOI layer near ends of drain and source areas through insulating layer
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ); IWAMATSU T (IWAM-I); MAEDA S (MAED-I); YAMAGUCHI Y (YAMA-I)
Inventor: IWAMATSU T; MAEDA S; YAMAGUCHI Y
Number of Countries: 020 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9822983	A1	19980528	WO 96JP3369	A	19961115	199827	B
EP 948057	A1	19991006	EP 96938489	A	19961115	199946	
			WO 96JP3369	A	19961115		

Abstract (Basic): WO 9822983 A
An SOI layer (5) is formed on a **silicon** substrate (1) with a **buried insulating** layer (3) in between. In the SOI layer (5), **SOI-MOSFET** having a drain area (5a) and a source area (5b) which are so formed as to define a channel forming area (5c) and a gate electrode layer (9) facing to the channel forming area (5c) with an insulating layer (7) in between is formed. There is provided an FS isolation structure in which an FS plate (11) which faces to the area of the SOI layer (5) near the ends of the drain and source areas (5a

and 5b) through the insulating layer (7) is provided and the **SOI-MOSFET** is electrically isolated from other elements by fixing the potential at the area of the SOI layer (5) facing the plate (11) by imparting a predetermined potential to the FS plate. The channel forming area (5c) has two end sections in the channel width direction and a central part between both end sections, and the channel length of the area (5c) in the end sections of the area (5c) is shorter than that in the central part.

Dwg.0/39

12/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010804842
WPI Acc No: 1996-301795/199631
XRPX Acc No: N96-253960
Semiconductor device with thin film **silicon** on insulator MOSFET - has impurity layer with high concn. in semiconductor substrate formed below **buried insulation** layer with MOSFET channel and source-drain regions formed above **buried insulation** layer
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: EIMORI T; MATSUFUSA J; OASHI T; NISHIMURA T
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19548076	A1	19960627	DE 1048076	A	19951221	199631	B
JP 8181316	A	19960712	JP 94319684	A	19941222	199638	
TW 297941	A	19970211	TW 95102322	A	19950311	199721	
CN 1130808	A	19960911	CN 95119435	A	19951221	199801	
US 5721444	A	19980224	US 95576352	A	19951221	199815	
			US 97824550	A	19970325		

Abstract (Basic): DE 19548076 A

The semiconductor device includes a substrate (1b) with a main surface in which is formed a **buried insulation** layer (2) in a position separate from the main surface. Also provided is a LOCOS insulating film (3b), a thin film transistor, and an impurity layer (15). The LOCOS film is provided in the main surface of the semiconductor substrate to insulate one active region from another active region.

The thin-layer transistor is formed in the active region and it has a gate electrode (8) on one active region with an intermediate gate insulating layer (7). Also provided is a pair of source/drain layers (5) in the substrate main surface on both sides of the gate electrode, and a channel region (4). The impurity layer is formed in the substrate with a high concentration impurity and it is directly under the buried layer. Pref. the thin-layer transistor is of planar or mesa type.

USE/ADVANTAGE - For DRAM with large capacity, e.g. 256 M, or logic circuit. Thin-film **SOI-MOSFET** prevents generation of ''buckel'' current, or current in OFF state due to weaker inversion region being provided by work function between impurity layer and MOSFET channel region.

12/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009997898
WPI Acc No: 1994-265609/199433
XRAM Acc No: C94-121450
XRPX Acc No: N94-209043
Silicon@-on-insulator semiconductor device - comprises forming pad oxide on wafer, forming oxynitride region etc. giving channel length region independent to channel width
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: RHEE T P; LEE T; RHEE T
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 612103	A2	19940824	EP 94301086	A	19940215	199433	B
TW 228609	A	19940821	TW 94101676	A	19940228	199436	
JP 6252403	A	19940909	JP 9418099	A	19940215	199441	
CN 1095860	A	19941130	CN 94102697	A	19940217	199547	

Abstract (Equivalent): US 5482877 A
A method for making a semiconductor device having a **silicon** -on-insulator, gate-all-around structure comprises forming a pad oxide on a wafer which includes a lower **silicon** substrate, a **buried insulator** layer, and an upper **silicon** layer; forming an oxynitride region on a portion of the **buried insulator** layer; forming an active **silicon** layer to intersect the oxynitride region; forming a cavity by wet-etching the exposed oxynitride region; forming a gate insulating layer on the surface of the exposed active **silicon** layer; depositing **polysilicon** to fill the cavity surrounding the active **silicon** layer; removing a portion of the **polysilicon** to form a gate electrode; and forming source and drain regions on the active **silicon** layer sepd. by the gate electrode.

12/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009217490
WPI Acc No: 1992-344912/199242
XRAM Acc No: C92-153310
XRPX Acc No: N92-262911
Forming **buried insulation** film in **silicon@**-substrate - by flattening **silicon@-silicon** dioxide interface by injecting oxygen ion and obtaining uniform characteristic of complete depletion layer type **SOI MOSFET** NoAbstract
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 4249323	A	19920904	JP 9114580	A	19910205	199242	B

Priority Applications (No Type Date): JP 9114580 A 19910205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 4249323	A		5	H01L-021/31	

12/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009049448
WPI Acc No: 1992-176821/199222
XRAM Acc No: C92-081034
XRPX Acc No: N92-133402
SOI-field effect transistor - comprises **SOI-MOSFET** formed on thin **silicon**@ layer on insulator layer, which when operation only additional source-drain regions are depleted
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: NISHIMURA T; YAMAGUCHI Y
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 487220	A2	19920527	EP 91310089	A	19911031	199222	B
JP 4188633	A	19920707	JP 90314544	A	19901119	199233	
EP 487220	A3	19920729	EP 91310089	A	19911031	199335	
EP 487220	B1	19970102	EP 91310089	A	19911031	199706	
DE 69123950	E	19970213	DE 623950	A	19911031	199712	
			EP 91310089	A	19911031		

Priority Applications (No Type Date): JP 90314544 A 19901119
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 487220	A2	E	20	H01L-029/784	
JP 4188633	A		12	H01L-021/336	
EP 487220	B1	E	24	H01L-029/772	
Designated States (Regional): DE FR GB					
DE 69123950	E			H01L-029/772	Based on patent EP 487220
EP 487220	A3			H01L-029/784	

Abstract (Basic): EP 487220 A

Semiconductor device comprises: 300-1500 Angstrom semiconductor layer (3) formed on an insulator (2), gate electrode (5) on the semiconductor with a gate insulating film (4) interposed between them. Pair of additional source/drain regions (7a,8a) of first conductivity type formed from immediately below both of the left and right side ends of the gate inward to immediately below the gate. Channel forming region (6) of second conductivity type (6) in a region between the additional source/drain regions. Pair of source/drain regions (7b,8b) of the first conductivity type formed adjacent to the ends of (7a) and (8a) and contacting channel (6).

Additional source/drain regions (7a,8a) have an impurity concn. of 3 x 10 power(17) - 3 x 10 power(18) cm3 and lower than (7b,8b).

Channel forming region (6) pref. has a first conductivity type impurity concn. of 10 power(16) - 10 power(17) cm3 and regions (7b, 8b) has a second type impurity 10 power(19) - 10 power(20) cm3. **Si** layer (3) is 1000-1500 Angstrom thick and additional source/drain regions (7a,7b) have second conductivity type impurity 3 x 10 power(17) - 5 x 10 power(17) cm3. Insulator (2) includes **silicon oxide** film formed as **buried** by implanting oxygen ions. Semiconductor layer (3) is a **Si** layer formed in a shape of an island on insulator (2). Channel forming region (6) is a p-type region including B, (7a,8a) are n-type including P and (7b,8b) are n-type including P or As.

12/3,AB/12 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07002806
SOI MOSFET DEVICE AND MANUFACTURING METHOD THEREOF

PUB. NO.: 2001-230423 [JP 2001230423 A]
PUBLISHED: August 24, 2001 (20010824)
INVENTOR(s): KAA HIN FUN
APPLICANT(s): INTERNATL BUSINESS MACH CORP (IBM)
APPL. NO.: 2001-000078 [JP 20011000078]
FILED: January 04, 2001 (20010104)
PRIORITY: 00 481914 [US 2000481914], US (United States of America), January 12, 2000 (20000112)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **SOI MOSFET** device having a buried metal body contact so as to improve performance and to reduce a size.

SOLUTION: A buried metal via is disposed right under a body region and is aligned with a gate. A buried metal is in contact with a body region but is not in contact with a source or a drain. This structure includes a metal interconnection right under a device in which one or a plurality of interconnection layers are in contact with a **silicon** insulating film from under the device via a **buried oxide** film. In this manner, the bottoms of the source of drain diffusion regions and body regions are also connected. Further, also a metal multilayer can be formed under the device by this structure, whereby packing density and performance can be improved.

12/3,AB/13 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06691907
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-277737 [JP 2000277737 A]
PUBLISHED: October 06, 2000 (20001006)
INVENTOR(s): PIDIN SERGEI
APPLICANT(s): FUJITSU LTD
APPL. NO.: 11-080161 [JP 9980161]
FILED: March 24, 1999 (19990324)

ABSTRACT

PROBLEM TO BE SOLVED: To enable suppression of a short channel effect, even when a channel length is short, by regulating the effective channel length of a transistor, on the basis of a specific formula having parameters of the thickness of a **buried insulating** film, the thickness of a semiconductor layer and the thickness of a gate insulating film.

SOLUTION: On a **silicon** substrate 10, a **buried insulating**

film 12 of a film thickness tBOX. an SOI layer 14 of a film thickness tSI. a gate insulating film 20 of a film thickness tFOX and a gate electrode are laminated successively. In parts of the SOI layer 14 on both sides of the gate electrode 22, a source diffusion layer 16 and a drain diffusion layer 18 are formed respectively. In this way, a complete depletion **SOI-MOSFET** is formed. Each parameter constituting the **SOI-MOSFET** is represented in a formula, by representing the effective channel length of the MOSFET as L, permittivity of **silicon** as ε **SI**. and permittivity of a **silicon** oxide film as εOX. In this way, the parameter of the **SOI-MOSFET** are set.

12/3,AB/14 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06427302
SEMICONDUCTOR DEVICE AND MANUFACTURE OF THE SEMICONDUCTOR DEVICE

PUB. NO.: 2000-012865 [JP 2000012865 A]
PUBLISHED: January 14, 2000 (20000114)
INVENTOR(s): MIYAMOTO SHOICHI
HIRANO YUICHI
IPPOSHI TAKASHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 10-174651 [JP 98174651]
FILED: June 22, 1998 (19980622)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a **SOI/MOSFET**, which does not have parasitic elements on the end parts of a **silicon** on insulator(SOI) layer.

SOLUTION: A SOI substrate 30 is provided with a **buried oxide** film 2, a SOI layer formed on a first region 51 in the surface 2S of the film 2 and a **silicon** oxide film 3, formed on a second region 5 in the same surface 2S. A **silicon** oxide film 6 is formed on the peripheral edge part of the layer 3, and the side surfaces 6H of the film 6 are coupled integrally with the side surfaces 8H, which are adjacent to the side surfaces 6H, of the film 8. The film thickness of the peripheral edge part of the layer 3 is formed smaller towards the film thickness heads for the end parts 3H of the layer 3, and the film thickness of the peripheral edge part of the film 6 is formed thicker towards the film thickness heads for the end parts 3H of the layer 3. A gate oxide film 10 is formed on the surface of the film 9 and on a part, which is formed integrally with the film 9 within the film 6, of the film.

12/3,AB/15 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05300346
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 08-255846 [JP 8255846 A]
PUBLISHED: October 01, 1996 (19961001)
INVENTOR(s): ASAI SHOKI
TSURUTA KAZUHIRO
APPLICANT(s): NIPPONDENSO CO LTD [000426] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-058371 [JP 9558371]
FILED: March 17, 1995 (19950317)

ABSTRACT

PURPOSE: To simplify a process for manufacturing a semiconductor device provided with a non-volatile memory and to flatten the surface of the device.

CONSTITUTION: An **SOI-MOSFET** 6 has such a structure that a source/drain is formed on an SOI layer 3B provided to a **silicon** substrate 1 through the intermediary of a **buried oxide** film 2, and a gate oxide film 4B and a gate electrode 5B are provided onto the source/drain. A MOSFET 7 used for a memory is composed of a source/drain formed on a **silicon** substrate 1, a **buried oxide** film 2 and the gate oxide film 2A formed at the same time, an SOI layer 3B and a floating gate 3A of single crystal semiconductor layer provided concurrently, and furthermore a gate oxide film 4B, a gate electrode 5B, an insulating film 4A, and a control gate 5A formed at the same time respectively.
? T S12/3,AB/16

12/3,AB/16 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

04056404
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 05-048104 [JP 5048104 A]
PUBLISHED: February 26, 1993 (19930226)
INVENTOR(s): MAKINO TAKAMI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-198182 [JP 91198182]
FILED: August 08, 1991 (19910808)
JOURNAL: Section: E, Section No. 1390, Vol. 17, No. 344, Pg. 97, June 29, 1993 (19930629)

ABSTRACT

PURPOSE: To enable a semiconductor device to have a low S/D diffusion layer resistance and contact resistance by forming a buried gate type back gate electrode and an S/D diffusion layer area on the surface of the back gate electrode opposite to a channel area.

CONSTITUTION: A signal-crystal **silicon** layer is formed as the facing channel area 37 of a gate electrode (back gate electrode) 26 **buried** in an **insulator** film 34 above the electrode 26 with the film 34 in between. Then another signal- crystal **silicon** layer, the source (S) and drain (D) of which are faced to the side faces of the electrode 26 with the film 34 in between and respectively constitute diffusion layers 32 and 33, is formed. In other words, the S and D high-concentration diffusion layers 32 and 33 are extended to the areas facing the side faces of the

back gate electrode layer 26. Therefore, the S/D diffusion layer resistance is lowered. Moreover, a dual-gate **SOI MOSFET** having sufficiently low contact resistance is obtained.

18/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013733113
WPI Acc No: 2001-217343/200122
XRPX Acc No: N01-154839
Silicon-on-**insulator metal oxide semiconductor** transistor structure, for integrated circuit, has contact area extending through **insulating layer**, for connecting either source, **drain** or **channel** with copper layer
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: HOLST J C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6153912	A	20001128	US 99427139	A	19991025	200122	B

Abstract (Basic): US 6153912 A
Abstract (Basic):
NOVELTY - An **insulating layer** (104) and semiconductor layer with **channel** area (114) formed between source (110) and **drain** (112), are sequentially formed on conductive copper layer (106). A conductive **gate** area (118) is formed on **channel** area. A contact area (120) extends through **insulating layer** , for electrically connecting either source, **drain** or **channel** with the copper layer.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **silicon**-on-insulator circuit.

18/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013538739
WPI Acc No: 2001-022945/200103
Related WPI Acc No: 1996-115715; 1997-118300; 2000-012292
XRAM Acc No: C01-006814
XRPX Acc No: N01-017827
Fabrication of a field effect transistor in a **silicon** layer involves forming **source** and **drain regions** with **channel** regions in the **silicon** layer using the **polysilicon gate** electrode as a dopant mask
Patent Assignee: UNIV CALIFORNIA (REGC)
Inventor: CHAN M J; HU C; KO P K; WANN H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6121077	A	20000919	US 94224363	A	19940407	200103	B
			US 95461355	A	19950605		
			US 99393767	A	19990910		

Div ex patent US 5982003

Abstract (Basic): US 6121077 A
Abstract (Basic):
NOVELTY - A field effect transistor in a **silicon** layer is fabricated by forming **source** and **drain regions** with

channel regions in the **silicon** layer using the **polysilicon gate** electrode as a dopant mask for self-alignment.

DETAILED DESCRIPTION - Fabrication of a field effect transistor in a **silicon layer** over an **insulating layer** comprises forming a **silicon oxide layer** on the **silicon** layer, forming a **silicon** nitride layer (46) on the **silicon oxide layer**, removing a portion of the **silicon** and the **silicon** nitride layer to expose a portion of the **silicon** layer, oxidizing the portion of **silicon** layer to form a thick **oxide layer** and thin the **silicon** layer to form a recessed portion, removing a portion the thick oxide to expose the recessed portion, growing a **gate** oxide (56) on the recessed portion, depositing **polysilicon** (52) on the **gate** oxide and on the **silicon** nitride layer, removing the **polysilicon** overlying the **silicon** nitride layer to leave a **polysilicon gate** electrode on the **gate** oxide, and forming **source** and **drain regions** (54, 55) in the **silicon** layer using the **polysilicon gate** electrode as a dopant mask for self-alignment.

18/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012460551
WPI Acc No: 1999-266659/199923
XRPX Acc No: N99-198907

Silicon on **insulator metal oxide semiconductor** transistor - has injection extension area with high doping concentration compared to that of impurity injection area

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KANG W; KANG W T
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10321871	A	19981204	JP 98126555	A	19980511	199923	B
KR 98082916	A	19981205	KR 9718022	A	19970509	200006	
CN 1204158	A	19990106	CN 98114959	A	19980509	200007	

Abstract (Basic): JP 10321871 A

NOVELTY - An N-type injection extension area is formed between each of P-type **diffusion** extension **areas** (114a,114b) and impurity injection **area**. An impurity **diffusion area** is adjoined to the injection extension area via a PN junction. The injection extension area have high doping concentration compared to that of impurity injection area. DETAILED DESCRIPTION - P-type **diffusion** extension **areas** (114a,114b) formed on both ends of impurity injection area has low doping concentration compared to impurity **diffusion area**. An **insulating layer** and element formation area are formed on the main surface of semiconductor. A semiconductor layer of thickness 1400 Angstrom or more is formed on the **insulating layer**. A P-type **channel** area (104) is formed at the bottom of element formation **area**. The impurity **diffusion area** is formed across **channel** area. A **gate** electrode (108) formed in-between **gate** oxide which is formed on **channel** area. An INDEPENDENT CLAIM is also included for manufacturing method of **silicon** on **insulator metal oxide semiconductor** (SOIMOS) transist

18/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011822318
WPI Acc No: 1998-239228/199821
XRAM Acc No: C98-074661
XRPX Acc No: N98-189218
Fully self-aligned **SOI MOSFET** production - involves forming relatively thin **channel** region that can be fully depleted to provide high current gain
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: AJURIA S; LUTZE J; POON S; VENKATESAN S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5736435	A	19980407	US 95497317	A	19950703	199821	B

Abstract (Basic): US 5736435 A
Production of a MOSFET comprises (i) forming isolation regions in a **silicon (Si) layer** overlying an **insulating layer** (12) on a single crystal **Si** body (10), to define an **active region**, (ii) planarising the isolation regions (16, 18) and the **active region**, (iii) forming a masking layer (22) having openings (24) on the planar surface, (iv) forming a recess in the **active region**, (v) forming a **gate** electrode (36) in the **Si** body, (vi) forming a **gate dielectric layer** in the recess, (vii) depositing a **gate** electrode forming material to fill the recess, (viii) planarising the **gate** electrode forming material to form a second **gate** electrode overlying the **gate dielectric layer**, (ix) forming an opening through the second **gate** electrode and the **insulating layer**, (x) forming a refractory **metal** plug (52) in the opening to electrically couple the first **gate** electrode to the second **gate** electrode, and (xi) forming **source** and **drain regions** (40, 42) in the **active region** on either side of the second **gate** electrode defining a **channel** region (44), the first **gate** electrode being separated from the **channel** region by the **insulating layer**.

18/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010030119
WPI Acc No: 1994-297832/199437
XRAM Acc No: C94-135633
XRPX Acc No: N94-234434
MOSFET with SOI structure - uses **metal** electrode to store up negative charges in **polysilicon@** layer
Patent Assignee: NIPPONDENSO CO LTD (NPDE)
Inventor: ASAI A; FUJINO S; HIMI H; TSURUTA K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6224433	A	19940812	JP 93131864	A	19930602	199437	B
US 5488243	A	19960130	US 93160885	A	19931203	199611	

Abstract (Basic): JP 6224433 A

The MOSFET consists of a **silicon** wafer (1) on top of which **insulation layer** (2) composed of SiO is formed. On top this **insulation layer**, a single crystal **silicon** layer (3) is formed. N+ **polysilicon gate** (6) is formed in this single crystal **silicon** layer.

A **polysilicon layer** (4) for electrical **insulation** is implanted in **insulation layer**. A **metal** electrode (5) is formed at the back of **silicon** wafer. The negative charges carried are stored up in the **polysilicon** wafer, using **metal** electrode through voltage impression.

18/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008998002
WPI Acc No: 1992-125275/199216
XRAM Acc No: C92-058431
XRPX Acc No: N92-093681
SOI type field effect transistor - having improved characteristic due to prevention of over-etching of **source-drain region**
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: AJIKA N; YAMAGCHI Y; YAMANO T; YAMAGUCHI Y
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 480635	A	19920415	EP 91309095	A	19911003	199216	B
JP 4147629	A	19920521	JP 90271727	A	19901009	199227	
US 5341028	A	19940823	US 91770041	A	19911003	199433	
EP 480635	B1	19950809	EP 91309095	A	19911003	199536	
US 5444282	A	19950822	US 91770041	A	19911003	199539	

Abstract (Equivalent): US 5444282 A

Semiconductor device comprises a semiconductor **layer** over an **insulator layer**; a **channel** region of a 1st conductivity in semiconductor layer; 1st **source** and **drain regions** of 2nd conductivity adjacent **channel** region; a **gate** electrode above **channel** region with a dielectric in between; 1st sidewall spacers on left and right sidewalls of **gate** electrode; an etch-resistant **metal** layer outside area where sidewall spacers are formed; 2nd sidewall spacers outside 1st; 2nd **source** and **drain regions** of high concn. than 1st outside 2nd sidewall spacers; and interconnection layer connected to **metal** layer. The **metal** layer is of cobalt silicide.

18/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008278490
WPI Acc No: 1990-165491/199022
XRAM Acc No: C90-072155
XRPX Acc No: N90-128466
Silicon-on-**insulator metal oxide semiconductor** with thin **film** FET - body region for improved withstand voltage between source and **drain**
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: NISHIMURA T; YAMAGUCHI Y
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 370809	A	19900530	EP 89312166	A	19891123	199022	B
JP 2144969	A	19900604	JP 88299136	A	19881125	199028	
US 5125007	A	19920623	US 89439680	A	19891122	199228	

Abstract (Equivalent): EP 370809 B
A MOS field effect transistor comprising: an insular substrate (2); a semiconductor layer (3) formed on said insulator substrate (2); a **channel** region (6) of a first conductivity type formed in said semiconductor layer (3); a **source region** (8) of a second conductivity type formed in said semiconductor layer (3) being in contact with one end of said **channel** region (6); a **drain** region (9) of the second conductivity type formed in said semiconductor layer (3) being in contact with the other end of said **channel** region (6); a body region (7) of the first conductivity type having a higher impurity concentration than that of said **channel** region (6) and being formed in contact with at least a part of a periphery of said **source region** (8) in said semiconductor layer (3); a **gate** electrode thin film (4) formed on said **channel** region (6); a **gate** electrode (5) formed on said **dielectric** thin **film** (4); a first conductor (14a) connected in common to said **source region** (8) and said body region (7); a second conductor (14b) connected to said **gate** electrode (5); and a third conductor (14c) connected to said **drain** region (9); which MOS field effect transistor is characterised in that: said body region (7) surrounds said **channel region** (6), said **source region** (8) and said **drain** region (9).

18/3,AB/8 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05992814
SEMICONDUCTOR DEVICE

PUB. NO.: 10-275914 [JP 10275914 A]
PUBLISHED: October 13, 1998 (19981013)
INVENTOR(s): KUMAGAI KOICHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-079381 [JP 9779381]
FILED: March 31, 1997 (19970331)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the layout area of a MOS field effect transistor(FET) by facilitating the fining of the **channel** length of the MOSFET shorter and, at the same time, to improve the degree of integration of a logic circuit.

SOLUTION: The manufacture of a MOSFET having a short **channel** length is made easier by constituting a **gate** 101 in a **silicon layer** on the **insulating layer** of an SOI(**silicon** -on-insulator)substrate, a **channel** region 103 and a **source** or **drain region** 104 in a **polysilicon** layer above the **gate** 101. The area of a **metallic** wiring area in a circuit block and the degree of integration of an element is improved by constituting such a circuit as the above-mentioned MOSFET on the same substrate as that of the **SOI MOSFET**.

18/3,AB/9 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05637330
SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 09-252130 [JP 9252130 A]
PUBLISHED: September 22, 1997 (19970922)
INVENTOR(s): YOSHIMI MAKOTO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-087722 [JP 9687722]
FILED: March 15, 1996 (19960315)

ABSTRACT

PROBLEM TO BE SOLVED: To provide an **SOI MOSFET** with a stable operation at high speed, by limiting over-shoot and holding a stable state in **drain** current of an SOI element even when a **gate** voltage is turned on and off continuously.

SOLUTION: Part of a single crystalline **silicon** layer 5 formed on an **insulating film** 3 on a semiconductor substrate 2 is diffused to form a substrate contact 6. **Source** and **drain regions** 11 and 12 are formed on the single crystalline **silicon** layer 5, and a main element 10 is formed on a substrate contact 6 with a second **insulating film** 7 in between. A switching element 20 is provided between the substrate contact 6 and a **drain** region 12. Then, conductance between a neutral region 16, located between the **source region** 11 and the **drain** region 12, and the substrate contact 6 is controlled by a depletion layer 22 at the single crystalline **silicon** layer 5. When the voltage applied to the **gate** is enough to make the **channel** of the main element 10 in a continuity state, the neutral region 16 and the high density **diffusion region** 6 are not in continuity state. When the voltage applied to the **gate** is enough to make the **channel** in a non- continuity state, the neutral region 16 and the **diffusion region** 6 are put in continuity state electrically.

18/3,AB/10 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05454810
INTEGRATED SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 09-069610 [JP 9069610 A]
PUBLISHED: March 11, 1997 (19970311)
INVENTOR(s): HISAMOTO MASARU
SHIBA TAKEO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-223412 [JP 95223412]
FILED: August 31, 1995 (19950831)

ABSTRACT

PROBLEM TO BE SOLVED: To simplify the formation of **SOI-MOSFET** in which there is no possibility of occurring of substrate floating by forming NMOSFET and PMOSFET in an **active area** of an SOI film and assigning a diffusion layer of the PMOSFET so as to be electrically connected to a **channel** of the NMOSFET.

SOLUTION: An **Si oxide film** 110 and a monocrystal **Si** film are formed on an **Si** substrate 120 for forming a SOI substrate. Then, with the use of the **Si oxide film** and an **Si** nitride film, an exposed part of the monacrystal **Si** film is oxidized for forming a thick **oxide film** 900 for element isolation, and then the **Si** nitride **film** and the **oxide film** are removed. Then, after a **gate oxide film** 910 is formed, a **gate** electrode 500 is formed. An N-type diffusion layer 300 of low resistance is formed with the **gate** electrode 500 and a specified mask pattern as masks, and a P-type diffusion layer 400 of low resistance is formed with the **gate** electrode 500 and another mask pattern as masks, and a wiring 700 connected to the N-type diffusion layer 300 and the P-type diffusion layer 400 is formed.

18/3,AB/11 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05198380
SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

PUB. NO.: 08-153880 [JP 8153880 A]
PUBLISHED: June 11, 1996 (19960611)
INVENTOR(s): SHIGYO NAOYUKI
TODA TOSHIYUKI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-240337 [JP 95240337]
FILED: September 19, 1995 (19950919)

ABSTRACT

PURPOSE: To suppress troubles caused by fine patterning, e.g. short **channel** effect, of an **SOI MOSFET**.

CONSTITUTION: An **insulation film**, i.e., a **silicon** oxide 102, is deposited on a p-type semiconductor substrate 101. A **drain** 104 of n(sup +) layer, similar to a source 103 of n(sup +) layer, is

provided on the **silicon** oxide 102 while spaced apart by a predetermined distance from a p-type substrate 110. An **insulation film**, i.e., a **silicon** oxide 106, is deposited on the **channel** part 105 between the source 103 and the **drain** 104 and a **gate** electrode 107 is formed on the **silicon** oxide. Heavily doped p-type regions 108, 109 are formed on the p-type semiconductor substrate 101 underlying the source 103 and the **drain** 104 formed on the p-type substrate (SOI layer) 110.

18/3,AB/12 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05052931
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 08-008431 [JP 8008431 A]
PUBLISHED: January 12, 1996 (19960112)
INVENTOR(s): TANAKA TORU
SUZUKI KUNIHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-134391 [JP 94134391]
FILED: June 16, 1994 (19940616)

ABSTRACT

PURPOSE: To provide an **SOI-MOSFET** wherein **channel** contact is enabled without causing the increase of junction capacitance and contact resistance, and stable voltage-current characteristics free from kink are obtained.

CONSTITUTION: A FET is formed in a **silicon film** on **insulator** . A transistor region 1 consists of a first region 1A and a second region 1B which are arranged in the **gate** width direction and a constricted part 1C which connects the regions 1A and 1B. A **source region** of a first conductivity type a **channel** region of a second or opposite conductivity type, and a **drain** region of the first conductivity type are formed in the first region 1A. A **gate** electrode 2 stretching as far as the constricted region 1C is formed on a **channel** region. A **channel** contact region composed of a diffused layer of the second conductivity type is formed in the second region 1B. As to the constricted region 1C, the width in the **gate** length direction is smaller than the width of the first region 1A, and a semiconductor device has a width greater than the **gate** length.

18/3,AB/13 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04725698
SOI-MOSFET AND MANUFACTURE THEREOF AND FORMING METHOD FOR ALIGNMENT MARK

PUB. NO.: 06-196698 [JP 6196698 A]
PUBLISHED: July 15, 1994 (19940715)
INVENTOR(s): HASHIMOTO MAKOTO
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-344811 [JP 92344811]
FILED: December 24, 1992 (19921224)

ABSTRACT

PURPOSE: To provide an **SOI-MOSFET**, in which a punch-through is inhibited and the increase of the capacitance of a **source region** and a **drain** region is suppressed, and manufacture thereof and the forming method of an alignment mark.

CONSTITUTION: An SOT-MOSFET has a **source region** 22, a **channel** region 23 and a **drain** region 24 formed in **silicon** , a surface **gate** electrode 20 formed to the upper section of the **channel** region 23, first **insulating films** 10 shaped under the regions of at least parts of the **source region** 22 and the **drain** region 24, a second **insulating film** 6 formed under the region of at least a part of the **channel** region 23 and a rear **gate** electrode 7 shaped under the first **insulating films** 10 and the second **insulating film** 6. The **film** thickness of the first **insulating films** 10 is made thicker than that of the second **insulating film** 6.

18/3,AB/14 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

03772457
MEMORY CELL

PUB. NO.: 04-137557 [JP 4137557 A]
PUBLISHED: May 12, 1992 (19920512)
INVENTOR(s): TSUCHIYA KENJI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-256963 [JP 90256963]
FILED: September 28, 1990 (19900928)
JOURNAL: Section: E, Section No. 1255, Vol. 16, No. 408, Pg. 99, August 28, 1992 (19920828)

ABSTRACT

PURPOSE: To ensure a sufficient capacitance and reduce the leak between **trenches** even in the case of small cell area, by constituting the **drain** bottom surface and the **trench** side wall of an **SOI MOSFET** , in a capacitor structure, and allowing a semiconductor substrate to serve as a cell plate.

CONSTITUTION: A **trench** 2 is formed on an N-type semiconductor substrate 1, and next an N-type region 3 of high concentration is formed. An **oxide film** 4 is formed, polycrystalline **silicon** 5 is deposited, phosphorus is diffused to increase concentration, and then etching-back is performed, thereby leaving the polycrystalline **silicon** 5 only in the **trench**. After amorphous **silicon** is deposited on the whole surface, it is fused by an electron beam and turned into single crystal **silicon** 6. An element isolation region 7 is formed. A **gate** electrode (word line) 8 of an **SOI MOSFET** is formed. After a source 9 and a **drain** 10 are formed, an interlayer **insulating film** 11, a bit line 12, an Al word line 13, etc., are formed. Thereby a sufficient capacitance can be ensured and the leak between **trenches** can be reduced.

18/3,AB/15 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

03443076
MOS FIELD-EFFECT TRANSISTOR

PUB. NO.: 03-105976 [JP 3105976 A]
PUBLISHED: May 02, 1991 (19910502)
INVENTOR(s): AOKI HIDEMITSU
MOGAMI TORU
OKABAYASHI HIDEKAZU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-244217 [JP 89244217]
FILED: September 19, 1989 (19890919)
JOURNAL: Section: E, Section No. 1094, Vol. 15, No. 295, Pg. 148, July 26, 1991 (19910726)

ABSTRACT

PURPOSE: To restrain a punchthrough and a short **channel** effect from being caused in a MOS field-effect transistor having a fine **gate** length by adopting the following: a limit curve which causes a short **channel** effect decided by a substrate concentration; the substrate concentration inside a region surrounded by a minimum value of a **drain** voltage and by a minimum value of an SOI film thickness; the SOI film thickness; and the **drain** voltage.

CONSTITUTION: In an n-Cb SOIMOSFET having a **gate** length of 0.1.mu.m, the following are set: a concentration of P-type impurities (boron) in a **channel** region in a **silicon** film is 5X10(sup 17)cm(sup -2); a concentration of N-type impurities (arsenic) in a source 4 and a **drain** 4' is 10(sup 20)cm(sup -3); a film thickness of a **gate oxide film** 2 is 5 nm; a material for a **gate** is n(sup +) poly-**Si**. In order to normally operate a device at a **drain** voltage of 1.0V or higher in the **SOI MOSFET**, an SOI film thickness must be 30nm and a substrate concentration must be 5X10(sup 17)cm(sup -2) or higher. By using an SOI structure in which the SOI film thickness and the substrate impurity concentration have been made optimum, it is possible to restrain a two-dimensional effect such as a punchthrough and a short **channel** effect.

18/3,AB/16 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03367471
SEMICONDUCTOR DEVICE

PUB. NO.: 03-030371 [JP 3030371 A]
PUBLISHED: February 08, 1991 (19910208)
INVENTOR(s): NISHIMURA TADASHI
INOUE YASUAKI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-164268 [JP 89164268]
FILED: June 27, 1989 (19890627)
JOURNAL: Section: E, Section No. 1059, Vol. 15, No. 159, Pg. 35, April 22, 1991 (19910422)

ABSTRACT

PURPOSE: To enhance the breakdown strength simultaneously obtaining the high current driving capacity during the miniaturization process of an SOI (**Silicon** On Insulation) structured MOSFET by a method wherein a low

impurity concentration diffused region is provided in a part of a single crystal **silicon** layer immediately beneath a **gate** electrode positioned on almost middle part between a **source region** and a **drain** region.

CONSTITUTION: The second conductivity type very narrow low impurity concentration diffused layer 5 is provided in a single crystal **silicon** layer immediately beneath a **gate** electrode 9 between **drain** .source 3a, 3b comprising the second conductivity type high concentration impurity diffused layer formed in a single crystal **silicon** layer formed on the first conductivity type **silicon** substrate 1 through the intermediary of an **insulating film** 2. Accordingly, the title semiconductor device is structured of two each of short **channel** MOSFET seriesconnected by providing an intermediate **drain** in a **gate** . Through these procedures, during the miniaturization process of a thin film **SOI/MOSFET** , the deterioration in breakdown strength can be avoided while obtaining the high current driving capacity.

20/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012784267
WPI Acc No: 1999-590493/199950
XRPX Acc No: N99-435482
Lateral thin film semiconductor-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) or diode
Patent Assignee: BASF AG (BADI); KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG); PHILIPS AB (PHIG)
Inventor: ARNOLD L D; CALDERWOOD D; FAFFERTY P; HIRST G C; JOHNSTON D N; MUNSCHAUER R; LETAVIC T; SIMPSON M
Number of Countries: 022 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5969387	A	19991019	US 98100832	A	19980619	199950	B
WO 9966539	A2	19991223	WO 99IB1004	A	19990603	200007	

Abstract (Basic): US 5969387 A
Abstract (Basic):
NOVELTY - A top oxide insulating layer (112) comprises a layer portion adjacent a channel region (106) which increases in thickness in a continuous manner in a direction from the channel region toward a drain region (108) over a distance of at least about a factor of five times greater than a maximum thickness of a thin semiconductor film (104). A lateral drift region (110) comprises a region portion adjacent the channel region which decreases in thickness in the same way.
DETAILED DESCRIPTION - The device includes a thin **buried oxide insulating** layer (102) on a semiconductor substrate. A lateral semiconductor device is provided in the thin semiconductor film on the thin **buried oxide**. The thin semiconductor film comprises the p-type channel region spaced from the n-type drain region by the n-type lateral drift region. The top oxide insulating layer is over the thin semiconductor film and a conductive field plate (114) is on the top oxide insulating layer. The device may be a diode or a MOSFET.

20/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06908296
METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

PUB. NO.: 2001-135821 [JP 2001135821 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): KOYAMA KAZUHIDE
APPLICANT(s): SONY CORP
APPL. NO.: 11-313231 [JP 99313231]
FILED: November 04, 1999 (19991104)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method for manufacturing a complete depletion type **SOI-MOSFET** which has an SOI layer thinned directly under a gate electrode and an SOI layer thickened in source and drain parts, using an SIMOX method and at the same time and shows a high

driving capability of the **SOI-MOSFET** in a self-aligned manner.

SOLUTION: The manufacturing method of a semiconductor device is provided with a process of forming a dummy gate 17 on a semiconductor substrate 11, a process of ion-implanting oxygen in the substrate 11, a process of heat-treating the substrate 11 to form a **buried oxide** film 18 in the region ion- implanted with the oxygen, a process of removing the gate 17 and a process of forming a gate electrode 44 on the region removed with the gate 17 via a gate insulating film 41.

20/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05430989
SEMICONDUCTOR DEVICE, AND ITS MANUFACTURE

PUB. NO.: 09-045789 [JP 9045789 A]
PUBLISHED: February 14, 1997 (19970214)
INVENTOR(s): KIMURA SHINICHIRO
HISAMOTO MASARU
MURAKAMI HIDEKAZU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-191757 [JP 95191757]
FILED: July 27, 1995 (19950727)

ABSTRACT

PROBLEM TO BE SOLVED: To provide an **SOI-MOSFET** where the potential of the SOI film can be fixed without increase of required and its manufacturing method.

SOLUTION: A heavily doped area 19 which has the first conductivity is provided in the specified section of the first conductivity type of SOI film 12 made on a **buried oxide** film 11, and the SOI film 12 is connected electrically to the semiconductor substrate 10 which has first conductivity, through a low resistance semiconductor 17 which has first conductivity, piercing the heavily doped area 19 and the **buried oxide** film 11. Hereby, the SOI film and the semiconductor substrate can be electrically connected with each other without providing special wiring, so specified potential can be applied to the SOI film with slight increase of area.

20/3,AB/4 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05123185
SOI-MOSFET AND ITS MANUFACTURE

PUB. NO.: 08-078685 [JP 8078685 A]
PUBLISHED: March 22, 1996 (19960322)
INVENTOR(s): SATO NORIAKI
KAWAI SHINICHI
ISHIGAKI TORU

APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-210021 [JP 94210021]
FILED: September 02, 1994 (19940902)

ABSTRACT

PURPOSE: To decrease leakage current between a source and the drain in a subthreshold region where gate voltage is low, without increasing the number of processes, by forming an opposite conductivity type overhanging region between the source and channel regions being the same conductivity type mutually.

CONSTITUTION: A SIMOX substrate is composed of a supporting substrate 1, a **buried oxide** film 2, and an SOI layer 3. And n-type overhanging regions 7 and 8 are formed by performing heat treatment in a nitrogen atmosphere, and diffusing and activating ion-implanted P. In a region interposed between the n-type overhanging regions 7 and 8, a p-type channel region 9 is formed. This opposite conductivity type overhanging region forms a potential barrier against carriers. Consequently, the channel region makes a mere resistor, and leakage current can be prevented from flowing between source and drain regions. Besides, this overhanging region can be formed without increasing the number of processes, by forming it simultaneously with other low- concentration regions of DDD structure.

25/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014151503
WPI Acc No: 2001-635722/200173
XRPX Acc No: N01-475549
Semiconductor device e.g. double **gate silicon** -ON-insulator-metal oxide **silicon** field effect transistor, has cavity formed on semiconductor substrate separating channel area and substrate
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001257358	A	20010921	JP 200069183	A	20000313	200173	B

Priority Applications (No Type Date): JP 200069183 A 20000313
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001257358	A		8	H01L-029/786	

Abstract (Basic): JP 2001257358 A
Abstract (Basic):
NOVELTY - A cavity (102) is formed on a semiconductor substrate, separating channel area and the substrate. **Gate insulating layer** (403) and **gate** electrode (401) are formed on the channel area.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device manufacturing method.
USE - Semiconductor device e.g. double **gate silicon**

25/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014107939
WPI Acc No: 2001-592151/200167
XRPX Acc No: N01-441158
Semiconductor device manufacturing method for e.g. MOSFET, involves substituting silicon group material layer exposed in group area with refractory material to form refractory metal **gate** electrode
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001024189	A	20010126	JP 99193932	A	19990708	200167	B

Abstract (Basic): JP 2001024189 A
Abstract (Basic):
NOVELTY - Protective layer (14) and **Si** material layer (13) formed on substrate (11) via **gate insulating film** (12) is patterned to **gate** shape. After forming SiO2 film at side walls of **gate** electrode, protective layer is etched and removed to form groove (16G), and exposes layer (13) which is substituted with refractory material to form refractory metal type layer and refractory metal type **gate** electrode (19G).
USE - For MOSFET, **SOI MOSFET**.

03/08/2002

25/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012964620
WPI Acc No: 2000-136471/200012
Related WPI Acc No: 2001-440152
XRPX Acc No: N00-102044
Electrostatic discharge protect device for IC chips like MOSFET chip
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: BROWN J S; GAUTHIER R J; VOLDMAN S H
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6015993	A	20000118	US 98144386	A	19980831	200012	B
KR 2000017399	A	20000325	KR 9934324	A	19990819	200104	
TW 428322	A	20010401	TW 99110334	A	19990621	200156	

Abstract (Basic): US 6015993 A
Abstract (Basic):
NOVELTY - High voltage tolerant diode (120) is formed with low doped **polysilicon gate film** (132) on **dielectric film** formed on semiconductor layer (124). The p and n-type doped regions (134,136) of **gate** film are shorted at surface by conducting layer (138) and as voltage is applied to film, it depletes. The depletable film is formed by counter-doping the **polysilicon**, or by low doped implantation of **polysilicon** film.
USE - For IC chips like MOSFET chip, **SOI-MOSFET** and diode based ESD networks. For mixed-voltage and mixed signal and analog/digital applications.

25/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012858293
WPI Acc No: 2000-030126/200003
XRAM Acc No: C00-007885
XRPX Acc No: N00-023150
Lamination structure of **SOI-MOSFET** array for semiconductor device manufacture - has partially empty **SOI-MOSFET** whose **gate oxide film**, SOI **layer** thickness and channel area impurity concentration are less than corresponding values of partially empty MOSFET
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE); IMAI K (IMAI-I)
Inventor: IMAI K
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11298001	A	19991029	JP 98104563	A	19980415	200003	B
CN 1232300	A	19991020	CN 99105730	A	19990413	200009	
KR 99083271	A	19991125	KR 9913606	A	19990414	200055	
US 6222234	B1	20010424	US 99288314	A	19990408	200125	

Abstract (Basic): JP 11298001 A
NOVELTY - On **silicon** substrate (1), partial empty type **SOI- MOSFET** (14) with channel area (NA2) and completely

empty type **SOI-MOSFET** (12) having SOI **layer** (3), **gate oxide film** (5) and channel area (NA1), are formed. The **film** thickness of **gate oxide film**, thickness of SOI layer and impurity concentration in channel area of completely empty MOSFET are smaller than corresponding values of partially empty MOSFET.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for lamination method of **SOI-MOSFET** array for semiconductor device.

USE - In **SOI-MOSFET** array for semiconductor device manufacture.

ADVANTAGE - Doping concentration control in channel areas is easy. MOSFET's with small difference in threshold voltages can be formed on the same substrate, even with reduced number of processes.

DESCRIPTION OF DRAWING(S) - The figure explains the process of lamination structure of **SOI-MOSFET** array. (1) **Silicon** substrate; (3) SOT **layer**; (5) **Gate oxide f**

25/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011020940
WPI Acc No: 1996-517890/199651
Related WPI Acc No: 1998-556563
XRAM Acc No: C96-162593
XRPX Acc No: N96-436449
Mfr of a body contact structure in an SOI device esp a MOSFET - by creating a heavily doped body contact region in an LDD region via implantation through a metal silicide layer
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: CHUNG S S; HSU C; LIANG M; WONG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5573961	A	19961112	US 95565201	A	19951109	199651	B

Abstract (Basic): US 5573961 A

SOI device is mfd by: growing field oxide (FOX) regions (4) on the SOI structure (3); growing first insulator layer (5) on non-FOX regions; adding overall poly-**Si** layer; implanting first-type dopant; patterning to form poly-**Si gate** (6); implanting second-type dopant into non-**gate** non-FOX regions (7); adding second **insulator layer** and etching to form insulating spacers (8) on the **gate** sidewalls; implanting first-type dopant through a resist mask into non-**gate** non-FOX regions (10); removing the mask; siliciding **Si** areas (11); removing unreacted metal; adding third **insulating layer** (12); opening contact holes (13) to the implanted first regions (10) and to a second SOI region (7); resist masking (14) to expose only the second region; implanting second-type dopant into the second region; removing the mask; annealing; and forming metal contacts (not shown) to the first and second regions.

25/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007354706
WPI Acc No: 1987-351712/198750
SOI-MOSFET type semiconductor unit - has monocrystal area formed on **insulation film**, and **gate** electrode through second **insulation film**, to avoid noise NoAbstract Dwg 1/7
Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 62254465	A	19871106	JP 8698608	A	19860428	198750	B

Priority Applications (No Type Date): JP 8698608 A 19860428
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 62254465	A		4		

25/3,AB/7 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07029724
SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 2001-257358 [JP 2001257358 A]
PUBLISHED: September 21, 2001 (20010921)
INVENTOR(s): TSUCHIAKI MASAKATSU
MIZUSHIMA ICHIRO
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 2000-069183 [JP 200069183]
FILED: March 13, 2000 (20000313)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device and its manufacturing method, which has the structure of an ultra high-speed double-**gate** **SOI-MOSFET** and can avoid the increase of its manufacturing cost and moreover satisfactorily receiving the increase of the mobility of its charged particles due to the double-**gate** **SOI-MOSFET** reduced to a thin film.

SOLUTION: After forming in a single-crystal **silicon** substrate a cavity 102 having an arbitrary shape, and while keeping intact the cavity portion, a lower **gate** **insulation** **film** 201 and the substance to be changed into a lower **gate** electrode 202 are formed on the inner wall surface of the cavity. Thereafter, the single-crystal **silicon** layer, present in the upper portion of the cavity, is processed in the form of an element region. At this time, an island-form single-crystal **silicon** layer constituting the element region is supported by the substance, to be changed into a lower **gate** electrode. Then, after processing and forming a first **gate** electrode on the element region, by using the first **gate** electrode as a mask, an impurity is so introduced selectively into the substance to be changed into the lower **gate** electrode as to be passed through the **silicon** layer which constitutes the element region. As a result, the

substance to be changed into the lower **gate** electrode is changed into an **insulation layer** in the region, other than the region masked by the first **gate** electrode.

25/3,AB/8 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06833204
FORMING METHOD OF **SILICON**-ON-INSULATOR BODY CONTACT AND BODY CONTACT STRUCTURE

PUB. NO.: 2001-060698 [JP 2001060698 A]
PUBLISHED: March 06, 2001 (20010306)
INVENTOR(s): MICHAEL J HAAGUROVU
MANDELMAN JACK A
APPLICANT(s): INTERNATL BUSINESS MACH CORP (IBM)
APPL. NO.: 2000-209836 [JP 2000209836]
FILED: July 11, 2000 (20000711)
PRIORITY: 351647 [US 99351647], US (United States of America), July 13, 1999 (19990713)

ABSTRACT
PROBLEM TO BE SOLVED: To form an SOI(**silicon**-on-insulator) structure substrate, having a body contact (a base-body contact) under a **gate** conductor.

SOLUTION: A **gate** conductor on SOI semiconductor structure is partitioned into segments, and the body contact is formed under the **gate** conductor segment. The body contact is formed by an opening. The opening is extended to a **silicon** substrate 22 through a TEOS **layer** 24, an SOI **layer** 18 and an **oxide layer** 20. A polysilicon layer 38, a TEOS layer 40 and a polysilicon layer 42 are formed at the opening. Charges stored from a body region under a **gate** can be removed rapidly by shaping the body contact, and a stable efficient **SOI MOSFET** can be realized.

25/3,AB/9 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06356393
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-298001 [JP 11298001 A]
PUBLISHED: October 29, 1999 (19991029)
INVENTOR(s): IMAI KIYOTAKA
APPLICANT(s): NEC CORP
APPL. NO.: 10-104563 [JP 98104563]
FILED: April 15, 1998 (19980415)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a semiconductor device provided with a

completely depleted MOSFET and a partially depleted MOSFET, both having satisfactory characteristics on the same substrate without controlling the impurity concentrations in channel regions and a method for manufacturing the device.

SOLUTION: This semiconductor device 10 is provided with a completely depleted **silicon**-on-insulator(**SOI**) **MOSFET** 12 and a partially depleted **SOI MOSFET** 14, which are separated from each other by a element separating film 4 on the same SOI substrate. The substrate has an embedded **oxide film** 2 and an SOI film 3 successively formed on a **silicon** substrate 1. The film thicknesses of the **gate oxide film** 5 and SOI layer 3 of the completely depleted **SOI MOSFET** 12 are made smaller than those of the **gate oxide film** 5 and SOI layer 3 of the partially depleted **SOI MOSFET** 14, and the impurity concentration in the channel region of the MOSFET 12 is made lower than that in the channel region of the MOSFET 14.

25/3,AB/10 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

06342597
FULLY INVERTED **SOI MOSFET**

PUB. NO.: 11-284201 [JP 11284201 A]
PUBLISHED: October 15, 1999 (19991015)
INVENTOR(s): SUGANO TAKUO
TOYABE TATSU
HANAJIRI TATSURO
IKEDA MIKI
APPLICANT(s): SUGANO TAKUO
TOYABE TATSU
HANAJIRI TATSURO
IKEDA MIKI
APPL. NO.: 10-121586 [JP 98121586]
FILED: March 27, 1998 (19980327)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a high-performance transistor which constitutes the next- generation semiconductor integrated circuit for which superhigh-density integration and extremely low power consumption are required.

SOLUTION: In a fully inverted **SOI MOSFET**, the termination of an electric force line from a **gate** in an ionized impurity in a space charge layer is eliminated by distinguishing the space charge layer by making a top **silicon** layer sufficiently thin and, in addition, the termination of the electric force line from the **gate** to substrate charges is suppressed by making the top **silicon layer** and an **insulating film** between substrates sufficiently thicker. Since the top **silicon** layer is made sufficiently thinner in the **SOI MOSFET**, the top **silicon** layer underlying the **gate** is set to an inverted state in which the space charge area is distinguished over the whole area of the top **silicon** layer when the transistor is operated and the control of channel charges by means of a **gate** electric field can be made more efficient. Consequently, an improvement of

characteristics, such as the suppression of short-channel effects, etc., can be expected from the transistor.

25/3,AB/11 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

02830974
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 01-128574 [JP 1128574 A]
PUBLISHED: May 22, 1989 (19890522)
INVENTOR(s): KAWAMURA SEIICHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-285438 [JP 87285438]
FILED: November 13, 1987 (19871113)
JOURNAL: Section: E, Section No. 809, Vol. 13, No. 378, Pg. 25, August 22, 1989 (19890822)

ABSTRACT

PURPOSE: To manufacture an **SOI/MOSFET** , in which integrated stray capacitance is decreased, by forming an **insulating layer** by laser recrystallizing SOI technology and O(sup +) ion implantation, and forming seeds in the device.

CONSTITUTION: Resist 3 is applied on an **insulating layer** 1. Then the resist 3 is patterned. With said resist 3 as a mask, windows 4 for seed parts A and B are provided by dry etching such as RIE. A part of a substrate is exposed. Single crystal parts are grown through the seed parts A and B with CW argon laser. A polycrystalline **silicon** layer 5 is recrystallized, and single crystal part is obtained. Then, O(sup +) ions are selectively implanted(I.I.) into upper parts C and D on the seed parts A at 400keV and 1.5X100(sup 18)/cm(sup 2). Thereafter, heat treatment is performed at a temperature of 1,250 deg.C for two hours in N(sub 2). **Insulating layers** 8 and 9 are continuously formed. Thus SOI(**Silicon** On Insulating Substrate) single crystal structure is obtained. Thereafter an **insulating layer** 10 is formed. Elements are isolated. Then the device is formed through the steps of an ordinary **SOI/MOSFET** (S.D.G is formed). A numeral 10 indicates a **gate** electrode.

32/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012924103
WPI Acc No: 2000-095939/200008
XRAM Acc No: C00-027888
XRPX Acc No: N00-074026
Junction forming device in **silicon**-on-**insulator metal oxide semiconductor** field effect transistor
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM I; KIM I G
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5998840	A	19991207	US 98148689	A	19980904	200008	B
KR 99024638	A	19990406	KR 9745863	A	19970904	200025	
US 6159778	A	20001212	US 99432029	A	19991029	200067	

Abstract (Basic): US 5998840 A
Abstract (Basic):
NOVELTY - A **metal** silicide layer having titanium disilicide is formed between electrically **insulating layer** and semiconductor region forming a non-rectifying junction with **source** and **channel region** of FET. The silicide layer ohmically contacts **source** and **channel regions** but does not form junction with **drain** region of FET. The electrically conductive layer is self-aligned to field oxide isolation region.
USE - In **silicon**-on-**insulator metal oxide semiconductor** field effect transistor.
ADVANTAGE - The refractory **metal** silicide layer provides highly conductive current path so that ohmic contact can be formed.

32/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012534003
WPI Acc No: 1999-340109/199929
XRAM Acc No: C99-100300
XRPX Acc No: N99-255037
Semiconductor device comprising an **SOI MOSFET**
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Inventor: ONISHI H
Number of Countries: 029 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 924773	A1	19990623	EP 98123767	A	19981214	199929	B
JP 11177103	A	19990702	JP 97362498	A	19971215	199937	
CN 1220496	A	19990623	CN 98123350	A	19981214	199943	

Abstract (Basic): EP 924773 A1
Abstract (Basic):
NOVELTY - Semiconductor device comprising an **SOI MOSFET** includes low-resistance source and **drain** electrodes formed of a high-melting **metal** silicide.
DETAILED DESCRIPTION - A semiconductor device comprises: an SOI substrate with a superficial thin **insulation film** and an upper thin silicon film; and a MOST comprising a first-type

channel, second-type **source/drain regions** diffused to the **insulation film**, high-melting **metal** silicide covering part of the **source/drain regions**, and a **polysilicon** layer formed between the **metal** silicide and the thin **insulation film**.

32/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04957168
MIS TYPE SEMICONDUCTOR DEVICE AND ITS FABRICATION

PUB. NO.: 07-249768 [JP 7249768 A]
PUBLISHED: September 26, 1995 (19950926)
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APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-042136 [JP 9442136]
FILED: March 14, 1994 (19940314)

ABSTRACT

PURPOSE: To achieve low cut-off characteristics and high driving capacity equivalent to those of a conventional complete depletion type **SOI MOSFET** while solving the essential problem i.e., lowering of withstand voltage of **drain** and hump or hystresis in the characteristics of element.

CONSTITUTION: The MIS type semiconductor device comprises a **source-drain region** provided in the semiconductor region 4 on the surface of a substrate 1 while being spaced apart from each other, a **channel** region formed in the **source-drain region** with protrusions and recesses being provided along a line connecting the **source** and **drain regions**, a first **insulating film** 2 embedded under the **channel** region while corresponding to the recess, a second **insulating film** 6 formed as a gate **insulating film** on the **channel** region, and a gate electrode 7 formed on the **channel** region through the second **insulating film** 6.

32/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03669880
SEMICONDUCTOR DEVICE

PUB. NO.: 04-034980 [JP 4034980 A]
PUBLISHED: February 05, 1992 (19920205)
INVENTOR(s): YAMAGUCHI YASUO
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APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-142155 [JP 90142155]

FILED: May 30, 1990 (19900530)
JOURNAL: Section: E, Section No. 1203, Vol. 16, No. 210, Pg. 71, May 19, 1992 (19920519)

ABSTRACT

PURPOSE: To manufacture an **SOI-MOSFET** in lessened substrate floating effect by a method wherein a part of the **insulating film** provided for separating the **SOI-MOSFET** is opened to provide the body contact for leading-out the surplus carrier.

CONSTITUTION: The surplus carrier as a **hole** in this NMOSFET generated by the collision ionization in the high field region at the interface between a **channel** region 8 and a **drain** region 10 runs into a well region 11 beneath **insulating films** 5 for separation passing through the **channel** region 8 beneath a gate electrode 5. At this time, the surplus carrier is led out of the system since the well region 11 is connected to a wiring layer 15 for body through the intermediary of a body contact 7. Accordingly, the **hole** can not be accumulated in the **channel** region 8 so as to lessen the so-called substrate floating effect. Through these procedures, the excellent transistor characteristics such as the restraint of the kink effect causing the constriction in the Id-Vd characteristics when the SOI film of an **SOI-MOSFET** is thicker and the deterioration in the breakdown strength between S/D when the SOI film is thinner can be displayed.
? T S32/3,AB/5-8

32/3,AB/5 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03669879
SEMICONDUCTOR DEVICE

PUB. NO.: 04-034979 [JP 4034979 A]
PUBLISHED: February 05, 1992 (19920205)
INVENTOR(s): KATO YUICHI
APPLICANT(s): SEIKO INSTR INC [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-143030 [JP 90143030]
FILED: May 30, 1990 (19900530)
JOURNAL: Section: E, Section No. 1203, Vol. 16, No. 210, Pg. 70, May 19, 1992 (19920519)

ABSTRACT

PURPOSE: To avoid the formation of a back **channel** for restraining the off leakage by isolating a source and a **drain** from an insulator.

CONSTITUTION: A gate **insulating film** 6 and a gate electrode 7 are provided on a **channel region** while a **source** 4 and a **drain** 5 are provided on both sides of the **channel** 3. At this time, the source 4 and the **drain** 5 must be formed to be isolated from an **insulating film** body 1. On the other hand, a depletion layer 9 as a **drain** must reach the underneath insulator 1. Accordingly, an **SOI- MOSFET** in the small **drain** capacity capable of rapid operations and in the low off leakage current due to the back **channel** formation can be manufactured.

32/3,AB/6 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03304871
SEMICONDUCTOR DEVICE

PUB. NO.: 02-280371 [JP 2280371 A]
PUBLISHED: November 16, 1990 (19901116)
INVENTOR(s): YAMAGUCHI YASUO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-102222 [JP 89102222]
FILED: April 20, 1989 (19890420)
JOURNAL: Section: E, Section No. 1030, Vol. 15, No. 50, Pg. 13, February 06, 1991 (19910206)

ABSTRACT

PURPOSE: To improve the breakdown voltage between a source and a **drain** by extending a **channel region** under the **source region** of an **SOI-MOSFET** and arranging a contact **hole** of the source so as to penetrate the **channel** region and providing a source electrode with a function as a substrate electrode.

CONSTITUTION: On an **insulator layer** 2 formed on a silicon substrate 1, an island-form semiconductor layer 3 made of a silicon thin film of 500 angstroms -1500 angstroms thick is formed, in which a first **channel** region 6 of P-type impurity concentration is formed. Also on both sides of said region 6 an in a lower part of the island 3, second **channel** regions 11 and 12 having high P-type impurity concentration are formed to be in contact with the region 6 eachly. The thickness of these regions 11 and 12 is about 1/2 of the island 3 and an additional **source region** 9 and an additional **drain** region 10 of 250 angstroms -1000 angstroms thick including N-type impurities are formed above the regions 11 and 12 so that these are in contact with the region 6. Furthermore, a first **source region** 7 and a first **drain** region 8 having a predetermined thickness are formed to be in contact with the regions 9 and 10 respectively, thereby forming an LDD structure.

32/3,AB/7 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03184267
MOS FIELD-EFFECT TRANSISTOR FORMED IN SEMICONDUCTOR **LAYER** ON **INSULATING** SUBSTRATE

PUB. NO.: 02-159767 [JP 2159767 A]
PUBLISHED: June 19, 1990 (19900619)
INVENTOR(s): YAMAGUCHI YASUO
KUSUNOKI SHIGERU
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-315807 [JP 88315807]
FILED: December 13, 1988 (19881213)
JOURNAL: Section: E, Section No. 975, Vol. 14, No. 414, Pg. 79, September 07, 1990 (19900907)

ABSTRACT

PURPOSE: To improve the breakdown strength between a source and a **drain** by a method wherein a first conductivity type carrier storing region whose impurity concentration is higher than that of a **channel** region is provided to a part of the **region** under a **source region** coming in contact with a part of the **channel** region.

CONSTITUTION: First conductivity type carrier storing regions 9a and 9b whose impurity concentrations are higher than that of a **channel** region 6 are provided to a part of the **region** under a **source region** 7 coming in contact with a part of the **channel** region 6. And, excessive first conductivity type carriers occurred in the **channel** region 6 by colliding electrons are removed from the **channel** region 6 and absorbed in the carrier storing regions 9a and 9b and stored. By this setup, a **SOI-MOSFET** can be improved in breakdown strength between a source and a **drain**.

32/3,AB/8 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02337565
SEMICONDUCTOR DEVICE

PUB. NO.: 62-254465 [JP 62254465 A]
PUBLISHED: November 06, 1987 (19871106)
INVENTOR(s): YAMADA TAKAHIRO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-098608 [JP 8698608]
FILED: April 28, 1986 (19860428)
JOURNAL: Section: E, Section No. 602, Vol. 12, No. 127, Pg. 158, April 20, 1988 (19880420)

ABSTRACT

PURPOSE: To enable a perfectly buried **channel** to be formed by a method wherein control electrodes are provided on the peripheral part of semiconductor region of **channel** forming region of an **SOI-MOSFET** through the intermediary of **insulating films**.

CONSTITUTION: An MOSFET T1 is composed of an n(sup +) **source region** 102, an n(sup +) **drain** region 103, an n **channel** region 104, a gate electrode 106 in an **insulating film** 105 formed in a thin film type single crystal region formed on an **insulating film** 101, a lower control electrode 107 provided in the **insulating film** 101 and an upper control electrode 108 provided on the peripheral part of **insulating film** 105. The upper and lower control electrodes 107, 108 can be formed of P type **polysilicon** or **metal** slightly impressed with standard negative voltage as a bias voltage. Through these procedures, a perfectly buried **channel** can be formed even if single crystal region is thin film type so that the movement and noise of elements may be markedly improved.